GAME CONDITION — QUICK REFERENCE — MALFUNCTION CODES

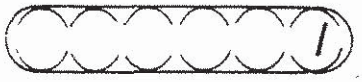
CODE	DESCRIPTION	CODE	DESCRIPTION
20	Coin switch jam	71	Spinning after indexing - Reel #1
30	Too many coins dispensed	72	Spinning after indexing - Reel #2
31	Hopper jam (Roller arm up too long)	73	Spinning after indexing - Reel #3
32	Hopper empty (Roller arm down too long)	74	Spinning after indexing - Reel #4
33	Reset occurred during payout	75	Spinning after indexing - Reel #5
41	Improper spin (Reel held, etc.) - Reel #1	91	Position error (2 of last 8 spins) - Reel #1
42	Improper spin (Reel held, etc.) - Reel #2	92	Position error (2 of last 8 spins) - Reel #2
43	Improper spin (Reel held, etc.) - Reel #3	93	Position error (2 of last 8 spins) - Reel #3
44	Improper spin (Reel held, etc.) - Reel #4	94	Position error (2 of last 8 spins) - Reel #4
45	Improper spin (Reel held, etc.) - Reel #5	95	Position error (2 of last 8 spins) - Reel #5
50	Door has been opened	For a detailed explanation see pages 20-23	
70	Illegal handle pull (No coins played) ; or	* This condition not applicable to games with a Replay Register or Atlantic City Models.	
70	Illegal game (Coins played, door open)*		

POWER UP MALFUNCTION CODES SERIES 1000

The M.P.U. Board Circuitry is configured in a way that directs the microprocessor to access an area of memory which is programed to conduct a brief self-test of basic circuit functions when power is applied.

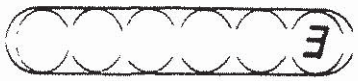
This is referred to as "Power Up Self Test." If during this test, the processor detects a circuit failure, it is programmed to output to the display a code indicating which circuit is at fault. The codes are as follows;

"Watch Dog" circuit failure



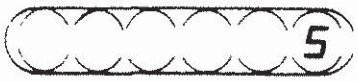
Ram failure Mode #1 (Normal)

Ram failure Mode #1 (Safe)

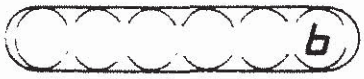


Incorrect or no second ROM

Incorrect or no third ROM



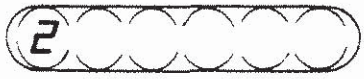
Incorrect PROM series



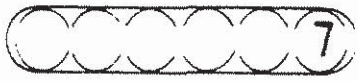
Memory test failure

For one second only, followed by:

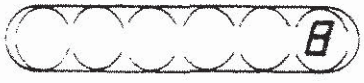
Example



Indicating which memory chip is at fault (M1, M2, M3 or M7)



No clocked interrupts



No zero crossing interrupts

Interrupt line (any) held low

The number of each test is displayed as above while the processor is preforming the test, but tests #1 thru #5 and #9 occur so quickly that the eye cannot detect them.